PHASE CHANGE MEMORY DEVICE EMPLOYING THERMALLY INSULATING VOIDS, AND A METHOD OF MAKING SAME

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FIELD OF THE INVENTION

The present invention relates to phase change memory devices, and more particularly to phase change memory devices employing thermally insulating voids.

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BACKGROUND OF THE INVENTION

There are many types of computer memory technologies that are presently used to store computer programs and data, including dynamic random access memory (DRAM), static random access memory (SRAM), erasable programmable read-only memory (EPROM), and electrically erasable programmable read only memory (EEPROM), etc.

15   Some memory technologies require electrical power to maintain the stored data (i.e. volatile memory), while others do not (i.e. non-volatile memory). Memory technologies can be read only, write once only, or repeatedly read/write.

There is an increasing demand for repeatedly read/write, non-volatile memory. The primary non-volatile memory technology presently used is EEPROM, which utilizes floating

20   gate field effect transistor devices each holding a charge on an insulated "floating gate". Each memory cell can be electrically programmed with a "1" or a "0" by injecting or removing electrons onto or from the floating gate. However, EEPROM memory cells are getting more difficult to scale down to smaller sizes, are relatively slow to read and program, and can consume a relatively large amount of power.

25   Phase change memory devices have also been known for some time. These devices use materials that can be electrically switched (programmed) between different structured states that exhibit different electrical read-out properties. For example, memory devices made of a chalcogenide material are known, where the chalcogenide material is programmed between a generally amorphous state that exhibits a relatively high resistivity, and a generally

30   crystalline state that exhibits a relatively low resistivity. The chalcogenide material is programmed by heating the material, whereby the amplitude and duration of the heating

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dictates whether the chalcogenide is left in an amorphous or crystallized state. The high and low resistivities represent programmed "1" and "0" values, which can be sensed by then measuring the resistivity of the chalcogenide material.

Fig. 1A illustrates a memory cell employing chalcogenide phase change memory material. The memory cell includes a layer of chalcogenide 2 disposed between a pair of electrodes 4/6, and over thermal insulator material 8. One of the electrodes (in this case the lower electrode 4) has an increased resistivity making it a thermal heater that heats the chalcogenide layer 2 when an electrical current is passed through the electrodes 4/6 (and through the chalcogenide layer 2). Fig. 1A, for example, shows the chalcogenide 2 in its crystallized form in which the material is highly conductive, and provides a low resistance between electrodes 4/6. When heated by electrode 4 by an amorphousizing thermal pulse, at least a portion 10 of the chalcogenide layer 2 is amorphousized, as shown in Fig. 1B, which increases the electrical resistance of the chalcogenide material. The chalcogenide 2 can by crystallized back to its lower electrical resistance state by applying a crystallization thermal pulse. The electrical resistance of this memory cell can be read using a small electrical current that does not generate enough heat to reprogram the chalcogenide material.

Phase change memory devices have a high program speed (e.g. 200 ns), and exhibit great endurance and program retention. It is even possible to program the phase memory material with varying degrees of amorphousization and thus varying degrees of resistivity, for selecting from three or more values to store in a single memory cell (multi-bit storage).

There is a constant need to shrink down the size of the memory cells. The power needed to program such memory cells is generally proportional to the cross-sectional area and volume of the memory material being amorphousized/crystallized. Thus, reducing the size and volume of the memory material used in each cell reduces the electrical current and power consumption of the memory device. Smaller sized memory cells also means smaller memory arrays, and more space between memory cells for thermal isolation.

Phase change memory devices are typically made by forming blocks of the memory material in holes etched into silicon materials. Thus, the resolution of the lithographic process used to make such holes dictates the dimensions of the memory material blocks in the memory cell. To shrink the cross-sectional area of the memory material blocks even

further, it is known to form spacers inside the holes before the memory material blocks are formed. See for example U.S. Patent 6,511,862, which teaches forming spacers over the heating electrode, and then filling the remaining space with a block of the memory material. While this technique reduces the width of the memory material block immediately adjacent

5   the heating electrode, it also results in the formation of the memory material block over just part of the heating electrode, which inefficiently transfers heat to the block of memory material using only part of the electrode's upper surface. This technique also fails to reduce the overall width of the memory cell, as well as effectively reduce the depth of memory material being programmed.

10   Shrinking the size of phase change memory cell arrays can also produce undesirable "program disturb" affects, which results when heat generated by one phase change memory cell affects the programming of phase change material in an adjacent memory cell. The program temperature of chalcogenide material can be as high as approximately 350 °C. Well known insulators used in most CMOS fabs (e.g. silicon oxide, silicon nitride, ILD, etc.) do

15   not provide sufficient thermal isolation in some applications to prevent the programming of one memory cell from inadvertently affecting the resistance of phase change material in an adjacent memory cell.

There is a need for a method and memory cell design that increases the heating efficiency of the memory cell, increases the thermal isolation between memory cells, while

20   reducing the size of the memory cells and the amount of memory material "programmed" by the heating process.

SUMMARY OF THE INVENTION

The present invention is a phase change memory device that includes a substrate, a

25   first electrode disposed over the substrate, phase change material disposed over and in electrical contact with the first electrode, a second electrode disposed over and in electrical contact with the phase change material, wherein electrical current passing through the first and second electrodes and the phase change material generates heat for heating the phase change material, and insulation material disposed adjacent to the phase change material,

wherein a void is formed in the insulation material to impede heat from the phase change material from conducting through the insulation material.

In another aspect of the present invention, a method of making a phase change memory device includes forming a first electrode over a substrate, forming phase change

5   material over the first electrode, forming a second electrode over the phase change material, wherein electrical current passing through the first and second electrodes and the phase change material generates heat for heating the phase change material, forming insulation material adjacent to the phase change material, and forming a void in the insulation to impede heat from the phase change material from conducting through the insulation material.

10   In yet another aspect of the present invention, a method of making a phase change memory device includes forming insulation material over a substrate, forming a hole in the insulation material, forming a first block of conductive material in the hole, forming a layer of phase change material in the hole and along at least a portion of an upper surface of the first block, forming a second block of conductive material in the hole and along at least a

15   portion of the phase change material layer, wherein electrical current passing through the first and second blocks and the phase change material layer generates heat for heating the phase change material layer, and forming a void in the insulation to impede the heat from the phase change material layer from conducting through the insulation material.

In yet one more aspect of the present invention, an array of phase change memory

20   devices includes a substrate, a plurality of first electrodes disposed over the substrate, phase change material disposed over and in electrical contact with the first electrodes, a plurality of second electrodes disposed over and in electrical contact with the phase change material, wherein electrical current passing through the first and second electrodes and the phase change material generates heat for heating the phase change material, and insulation material

25   disposed adjacent to the phase change material, wherein a plurality of voids are formed in the insulation material to impede heat from the phase change material from conducting through the insulation material.

In yet one additional aspect of the present invention, a method of making an array of phase change memory devices includes forming first electrodes over a substrate, forming

30   phase change material over the first electrodes, forming second electrodes over the phase

change material, wherein electrical current passing through the first and second electrodes and the phase change material generates heat for heating the phase change material, forming insulation material adjacent to the phase change material, and forming voids in the insulation to impede heat from the phase change material from conducting through the insulation

5   material.

.   Other objects and features of the present invention will become apparent by a review of the specification, claims and appended figures.

BRIEF DESCRIPTION OF THE DRAWINGS

10   Fig. 1A is a cross-sectional view of a conventional phase change memory device.

Fig. 1B is a cross-sectional view of the conventional phase change memory device, after undergoing an amorphousizing thermal pulse.

Figs. 2A to 2I are cross-sectional views illustrating the process of forming the phase change memory device of the present invention.

15   Fig. 2J is a top cross-sectional view of the phase change memory device of the present invention.

Fig. 3 is a graph illustrating amorphousizing and crystallization of the phase change memory material of the present invention.

Fig. 4 is a cross-sectional view of an alternate embodiment of the phase change

20   memory device of the present invention.

Fig. 5 is a cross-sectional view of a second alternate embodiment of the phase change memory device of the present invention.

Figs. 6A-6C are cross-sectional views illustrating the process of forming a third alternate embodiment of the phase change memory device of the present invention.

25   Fig. 6D is a top cross-sectional view of the third alternate embodiment of the phase change memory device of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is an improved phase change memory device, and method of

30   making such a device, where thermal isolation between memory cells is improved, the

volume of the phase change material programmed in the memory cell is reduced, and the heat

used to program the memory device is efficiently focused onto that volume of material using

a narrowing current path having a minimum cross-section adjacent that volume of material.

Figs. 2A to 2J illustrate the formation of the phase change memory cells of the

5   present invention. Fig. 1A illustrates well known MOS FET transistors 20, the formation of

which is well known in the art and not described herein in any detail. The MOS FET

transistors 20 each include a conductive gate 22 formed over and insulated from a silicon

substrate 24. Source and drain regions 26/28 (i.e. first and second regions that are

interchangeable) are formed in the substrate 24 and have a conductivity type (e.g. N type)

10   different from that of the substrate 24 (e.g. P type). The channel region 30 of the substrate is

defined between the source and drain regions 26/28, and is selectively made conductive

("turned on and off") by varying the voltage on gate 22. Insulation spacers 32 are formed

laterally adjacent to the gate 22, and are used to help form LDD (lightly doped) portions of

the source and drain regions 26/28, which is well known in the art . Gate 22 and spacers 32

15   are surrounded by insulation material 34, which is typically formed from one or more layers

of insulation materials (e.g. silicon dioxide -- "oxide", silicon nitride -- "nitride", ILD, etc.).

It should be noted that, as used herein, the terms "over" and "on" both inclusively

include "directly on" (no intermediate materials, elements or space disposed therebetween)

and "indirectly on" (intermediate materials, elements or space disposed therebetween).

20   Likewise, the term "adjacent" includes "directly adjacent" (no intermediate materials,

elements or space disposed therebetween) and "indirectly adjacent" (intermediate materials,

elements or space disposed therebetween). For example, forming an element "over a

substrate" can include forming the element directly on the substrate with no intermediate

materials/elements therebetween, as well as forming the element indirectly on the substrate

25   with one or more intermediate materials/elements therebetween.

Starting with the structure shown in Fig. 2A, a plurality of memory cells are formed

in the following manner, with each memory cell being formed adjacent to one of the

transistors 20. Contact holes 36 are formed into the insulation material 34 using a

lithographic etch process, where photo resist material 38 is formed over the insulation

30   material 34, and portions thereof are removed to expose selected portions of the insulation

material 34. An anisotropic etch process follows, which removes the exposed insulation material 34 to form contact holes 36 that extend down to and expose the source regions 26 of the substrate 24. The resulting structure is shown in Fig. 2B.

5   After the photo resist 38 is removed, spacer material 40 is formed in the contact holes 36. Formation of spacers is well known in the art, and involves the deposition of a material over the contour of a structure, followed by an anisotropic etch process, whereby the material is removed from horizontal surfaces of the structure, while the material remains largely intact on vertically oriented surfaces of the structure. The upper surface of the spacer material curves downwardly in a generally rounded manner as it extends away from the structure

10   against which it is formed. Thus, when spacers are formed in holes, opposing portions of the spacer material extend toward each other creating a central opening having a width or diameter that decreases with depth (i.e. funnel shaped). Spacer material 40 can be formed of any dielectric material, such as oxide, nitride, ILD, un-doped polysilicon, etc. Preferably, the material used to form spacers 40 is etch-selective relative to insulation material 34. In the

15   present embodiment, spacer material 40 is formed of nitride by depositing a layer of nitride over the entire structure followed by an anisotropic nitride etch process, such as the well known Reactive Ion Etch (RIE), to remove the deposited nitride except for spacer material 40 formed along the sidewalls of contact openings 36, as shown in Fig. 2C. The spacer material defines an opening 37 having a width that narrows with depth, and is less than that defined

20   by the lithographic process that originally formed the contact holes 36 (e.g. by as much as 80% or more).

A thick layer of conductive material (e.g. tungsten, titanium-tungsten, etc.) is deposited over the structure, which fills the openings 37 in contact holes 36 with the conductive material. A CMP (chemical-mechanical polishing) etch follows using the top

25   surface of the insulation material 34 as an etch stop, which removes the conductive material except for blocks 42 thereof inside contact holes 36. A controlled etch process is then used to recess the tops of blocks 42 below the top surface of the insulation material 34, as illustrated in Fig. 2D. After the structure is cleaned to remove all etch residue, polymers, etc., a thin layer of phase change memory material 44 (e.g. 5-200 nm thickness) is formed

30   over the structure, including inside openings 37 (along spacer material 40 and on blocks 42),

as shown in Fig. 2E. The preferred phase change material is a chalcogenide alloy, which includes at least one Group VI element (e.g. $Ge_2Sb_2Te_5$). For this embodiment, the layer of memory material 44 is preferably thin enough so that it does not merge together as a single vertical column in each contact hole 36 as it extends down to and covers block 42.

5   Another thick layer of conductive material (e.g. tungsten, titanium-tungsten, etc.) is deposited over the structure, filling openings 37 in contact holes 36. A CMP etch follows using the top surface of the insulation material 34 as an etch stop, which removes those portions of the conductive material and memory material 44 that are disposed outside of contact holes 36, and results in blocks 46 of the conductive material disposed in contact holes 10   36 and over memory material layer 44, as shown in Fig. 2F. The resulting structure preferably includes rows of memory cells 48 and their associated transistors 20. The conductive material used to form blocks 46 can be selected and/or doped (e.g. by ion implant or by in-situ process) for increased resistivity, to enhance the heat generated thereby during operation, as explained in further detail below.

15   The structure is then planarized (e.g. by a CMP etch) to expose top portions 40a of the spacers 40, as shown in Fig. 2G. An etch is then performed (e.g. if spacers 40 are nitride: an anisotropic hot phous-solution nitride etch; if spacers 40 are ILD: RIE etch; if spacers 40 are polysilicon: KOH etch) to remove the exposed portions of the spacers 40, creating voids (i.e. air gaps) 50 in spacers 40 that laterally surround the memory material 44. A poorly 20   conformal insulation layer 52 (e.g. ILD formed by fast deposition rate of PECVD) is formed over the structure so that the insulation material only slightly penetrates into (and otherwise does not fill) the voids 50, as shown in Fig. 2H. Layer 52 seals the voids 50, while providing mechanical strength to the structure adjacent the tops of voids 50.

An industry standard Cu-damascene CMP-based wiring process follows, which forms 25   nitride layer 54 over ILD layer 52, an ILD layer 54 over nitride layer 52, and metal contacts 54 (e.g. Cu) that extend down to and make electrical contact with the conductive blocks 46. The final structure is shown in Figs. 2I and 2J.

Fig. 2I shows a single memory cell 48, and its associated transistor 20. Blocks 42 and 46 constitute the memory cell's lower and upper electrodes, respectively, which are used to 30   program and read the memory material 44 therebetween. Upper electrode 46 has a width that

narrows as it extends down toward the lower electrode 42 (i.e. has a lower portion 46a that is narrower than an upper portion 46b). This narrowing of the electrode width is caused by the shape of the spacer material 40, against which the memory material layer 44 and upper electrode 46 are formed. The upper electrode 46 (and memory material layer 44 adjacent

5   thereto) define a narrowing current path for the memory cell 48 that reaches its smallest width at the thin layer portion 44a disposed directly above the lower electrode 42.

To program the memory cell 48, a voltage is applied across upper electrode 46 (via metal contact 58) and drain region 28, and a voltage is applied to gate 22 to turn on channel region 30 of transistor 20, so that an electrical current pulse of predetermined amplitude and

10   duration flows through transistor 20, lower electrode 42, memory material 44 and upper electrode 46. The electrical current pulse flowing through upper electrode generates heat, which is concentrated in the lower portion 46a thereof where there is the greatest current density. The generated heat in turn heats the memory material 44, and in particular the lower portion 44a thereof that is disposed between the narrowest portion of upper electrode 46 and

15   lower electrode 42. The memory material lower portion 44a is amorphousized or crystallized depending on the amplitude and duration of the electrical current pulse, as discussed below.

Fig. 3 is a graphical representation of how the layer 44 of chalcogenide phase change memory material (and in particular layer portion 44a thereof) is programmed with either a relatively high or relatively low resistivity. To amorphousize the chalcogenide memory

20   material, it is heated to a temperature beyond its amorphousizing temperature T_A. Once this temperature is reached, the volume of memory material is rapidly cooled by removing the electrical current flow. So long as the memory material is cooled faster than the rate at which it can crystallize, the memory material is left in a relatively high resistive amorphous state. To crystallize the memory material, it is heated beyond its crystallization temperature T_C, and

25   maintained above that temperature for a sufficient time to allow the memory material to crystallize. After such time, the electrical current flow is removed, and the memory material is left in a relatively low resistive crystallized state. It is also possible to vary the thermal pulse amplitude and duration to produce varying degrees of resistivity for multi-bit storage in a single memory cell.

To read the memory cell, an electrical current is passed through the memory cell that has an amplitude and/or duration that is insufficient to program the memory cell, but is sufficient to measure its resistivity. Low or high resistivities (corresponding to crystallized or amorphous states respectively of the memory material 44) represent digital "1" or "0"

5   values (or a range of resistivities representing multiple bits of data). These values are maintained by the memory cells until they are reprogrammed. The memory cells 48 are preferably formed in an array configuration, with the upper electrodes 46, drain regions 28 and gates 22 connected in row or column connection lines, so that each memory cell 48 can be individually programmed and read without disturbing adjacent memory cells.

10   Voids 50 are self aligned to the memory cell 48 (and to memory material 44 in particular) and provide additional thermal insulation. In particular, voids 50 help prevent the heat generated by memory cell 48 during programming from conducting through the surrounding insulation material and adversely affecting adjacent memory cells. Likewise, voids 50 help prevent heat generated by adjacent memory cells from reaching the phase

15   change material 44 of memory cell 48. In the embodiment shown in Fig. 2I, the void 50 is an annular-shaped trench that laterally surrounds the phase change material 44 to impede the lateral conduction of heat, as shown in the top view of Fig. 2J.

Insulation material 52 disposed at the tops of voids 50 seal such voids and prevent subsequent material processing from filling voids 50. Both the insulation material 52

20   disposed at the tops of voids 50 and the spacer material 40 disposed underneath voids 50 offer mechanical strength to the memory cell 48. Voids 50 are formed using standard CMOS processing and techniques (e.g. spacer formation, CMP etch, anisotropic etch, etc.), and using standard tooling, without introducing special, untested insulation materials.

Using spacers 40 to taper (narrow) down the width of heating electrode 46, and using

25   a thin layer of the programmable memory material disposed at the thin tip of the heating electrode 46, reduces both the width and depth of the programmed memory material in the memory cell, thus reducing the electrical current (and overall power consumption) needed to program the memory device. The narrowing current path defined by the upper electrode 46 produces a maximum current density, and therefore a maximum heat generation, directly

30   adjacent to the memory material to be programmed, which minimizes the amplitude and

duration of electrical current needed to program the memory device. Surrounding the heating

electrode 46 with spacers 40 also increases the distance (and therefore thermal isolation)

between heating electrodes and programming material layers from adjacent cells.

5   Fig. 4 illustrates an alternate embodiment of the present invention, where the lower

electrode 42 is formed before the formation of the spacers 40. In this embodiment, the lower

electrode width is not reduced by the spacers 40. This allows for the optional formation of an

indentation 60 into the upper surface of the lower electrode (e.g. by Ar sputtering on the

portion of lower electrode 42 left exposed by the spacer material 40 before the formation of

the memory material layer). This indentation 60 sharpens the tip of upper electrode lower

10   portion 46a, and better focuses the heat generation at the chalcogenide material 44a disposed

directly in-between this tip and the lower electrode 42.

           Fig. 5 illustrates a second alternate embodiment of the present invention, where the

thickness of the chalcogenide layer (compared to the area of the lower electrode 42 left

exposed by the spacer material 40) is great enough so that the chalcogenide layer merges to

15   define a narrow column 44b of the chalcogenide material directly over the lower electrode

42. The upper electrode 46 and chalcogenide layer 44 define a narrowing current path that

reaches a minimum width at the chalcogenide column 44b. With this embodiment, the

greatest current density in the memory cell 48 is found inside the chalcogenide column 44b.

Thus, the chalcogenide material that forms column 44b heats itself as current passes through

20   the memory cell. In fact, during an amorphousizing thermal pulse, as the chalcogenide heats

up and pockets of the chalcogenide material become amorphous, the resistivity of column

44b rises, causing even more heat dissipation within the column material.

           Figs. 6A-6D show a third alternate embodiment, to illustrate that the use of voids to

thermally isolate the memory cells is not limited to phase change memory cells having

25   narrowing current paths. Starting with the structure shown in Fig. 2B, a substantially

uniform layer of insulation material 62 is formed along the side walls of contact holes 36.

This can be done by forming spacer material in the manner described above with respect to

Fig. 2C, and then performing a planarization (e.g. CMP) etch to remove enough of the

structure so that only the vertically oriented portions of the spacer material remains, thus

30   leaving a layer of material 62 having a substantially uniform thickness along the contact hole

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sidewalls, as shown in Fig. 6A. This layer 62 is preferably formed of a material (e.g. nitride) that is etch-selective relative to insulation material 34 (e.g. ILD).

Lower electrode 42, phase change material 44 and upper electrode 46 are next formed using the processing disclosed above with respect to Figs. 2D-2F, resulting in the structure shown in Fig. 6B. The insulation etch for creating voids 50 as applied to layer 62, and the formation of the poorly conformal insulation layer 52, are performed using the processing disclosed above with respect to Fig. 2G, resulting in the structure shown in Fig. 6C. This structure corresponds to that shown in Fig. 2H, except that electrode 46 and phase change material 44 do not form a narrowing current path. Also, depending upon how deep the voids 50 are made, there may be no insulation material 62 in direct contact with the phase change material 44, where void 50 is an annularly shaped notch formed in the insulation material surrounding the phase change material 44 (i.e. void 50 is directly adjacent to the phase change material 44), as shown in Figs. 6C and 6D.

It is to be understood that the present invention is not limited to the embodiment(s) described above and illustrated herein, but encompasses any and all variations falling within the scope of the appended claims. For example, the contact holes 36 are preferably circular with annular spacer material 40 evenly formed about an open center. However, contact holes can take any shape (elongated, trench-like, elliptical, oval, etc.). The formation of the spacer material 40 can include several successive material deposition/etch processes, to narrow contact hole 36 down to any desired width/diameter. The transistor associated with each memory cell need not be disposed laterally adjacent the memory as shown in the figures, and could even be formed underneath the memory cell between the lower electrode and the substrate. While the upper electrode 46 and chalcogenide layer 44 are formed in opening 37 (and contact hole 36), at least some portions of these elements can extend out of opening/hole 37/36 as well. Materials, processes and numerical examples described above are exemplary only, and should not be deemed to limit the claims. As is apparent from the claims and specification, not all method steps need be performed in the exact order illustrated or claimed, but rather in any order that allows the proper formation of the memory cell of the present invention. Lastly, single layers of material can be formed as multiple layers of such or similar materials, and vice versa.